High Performance Computing

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Intro: HW vs SW

- The clock frequency of FPGA devices is typically one order of magnitude slower than the one of processors
  - 500 MHz vs 3 GHz
- However, FPGAs outperform at 3 key points:
  - Pipelining, Parallelism and Power
- It is difficult to maintain the pipeline of a processor continuously: full – data dependencies, cache misses, etc.
- Processors have a limited parallelism (4 to 8 functional units) that are usually poorly exploited due to compiler limitations
  - Parallelizing is still the Holy Grail of computing
- FPGA power is typically one or order of magnitude smaller
- Other important issue are the limitations of the general-purpose instruction sets
  - FPGAs are very good in algorithms with “strange” computations, e.g. cryptography.

Intro: Reconfigurable Computing

- Software is flexible and versatile... but slow
  - Provided that there is a compiler, a processor can execute any code (faster or slower, but will execute it)
  - Programs can be loaded and executed at run-time
- Pure hardware implementations lack flexibility
  - Hardware cannot be changed, unless is reconfigurable
- Use reconfigurable devices to execute an algorithm
  - Programmable logic devices, FPGAs in particular
- Bridge the gap between hardware and software
  - Speed of hardware
  - Flexibility of software

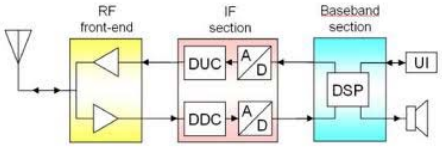
Intro: WH + SW synergy

- The idea is adding a reconfigurable device as a coprocessor to a conventional computing system
- There are different degrees of coupling between CPU and reconfigurable device
  - Functional unit inside the CPU (ASIPs, Application-Specific Instruction-set Processor)
  - CPU co-processor interface (Embedded systems)
  - Co-processing board (Desktop reconfigurable computing)
  - External processing unit
- Reconfigurable computing is about exploiting the synergy between hardware and software.
- Algorithm implementations have a SW and a HW part
  - Though the borders can be fuzzy sometimes, especially in those architectures where the reconfigurable array is tightly coupled.

RC Applications

- Classic RC application domains:
  - Scientific applications
  - Bioinformatics
  - Cryptography
  - Image processing

- Digital signal processing
  - Typically boards with A/D and D/A converters
  - Radar, Software-Defined Radio



- Embedded multimedia
  - Codec Acceleration
- Networking
  - Real-time analysis of network traffic (e.g. intrusion detection)

RC Applications

- All the previous applications have something in common: high performance.
  - HPRC (high performance reconfigurable computing)

Acceleration using HPRC

Applications	HW (FPGA)	SW Only
Hough & inverse Hough processing	2 seconds of processing time @20Mhz **370x faster**	12 minutes processing time Pentium 4 - 3Ghz
AES 1MB data processing/cryptography rate Encryption Decryption	424 ms/19.7 MB/s 424 ms/19.7 MB/s **13x faster**	5,558 ms / 1.51 MB/s 5,562 ms / 1.51 MB/s
Smith-Waterman ssearch34 from FASTA	100 sec FPGA processing **64x faster**	6461 sec processing time Opteron
Multi-dimensional hypercube search	1.06 Sec FPGA@140Mhz Virtex II **113x faster**	119.5 Sec Opteron - 2.2 Ghz
Monte-Carlo Analysis 64,000 paths	10 sec of Processing @200 Mhz FPGA system **10x faster**	100 sec processing time Opteron - 2.4 Ghz
BJM Financial Analysis 5 million paths	242 sec of Processing @61 Mhz FPGA system **26x faster**	6300 sec processing time Pentium 4 – 1.5 Ghz
Black-Scholes	18 msec FPGA@110Mhz Virtex-4 **203x faster**	3.7 Sec 1M iterations Opteron - 2.2 Ghz

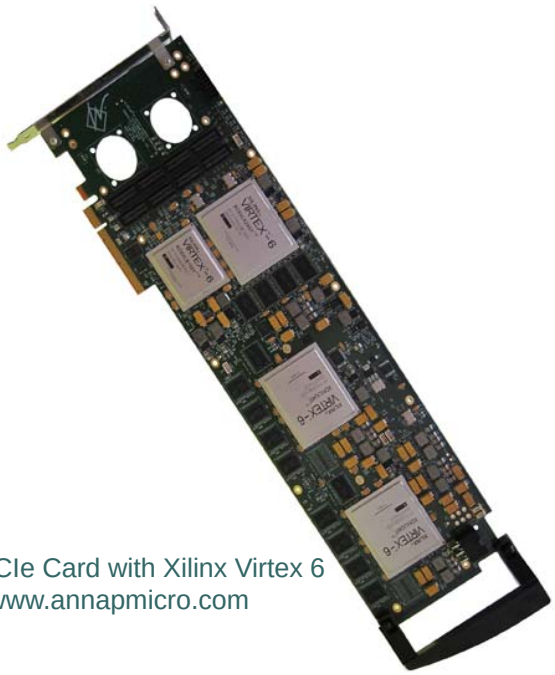
HPRC Platforms

- *Standalone systems*

- Accelerator connected by a high performance bus (PCIe, etc.)
- Accelerator directly connected to a high speed interprocessor bus such as Hiperlink or FSB (FrontSide Bus)

Reconfigurable Computing: Acceleration Boards

- FPGA co-processing boards for a desktop computer
  - PCIe and Hypertransport boards
- There are two main bottlenecks
  - I/O Bandwidth
  - Local memory



WILDSTAR 6 PCIe Card with Xilinx Virtex 6 FPGAs - http://www.annapmicro.com

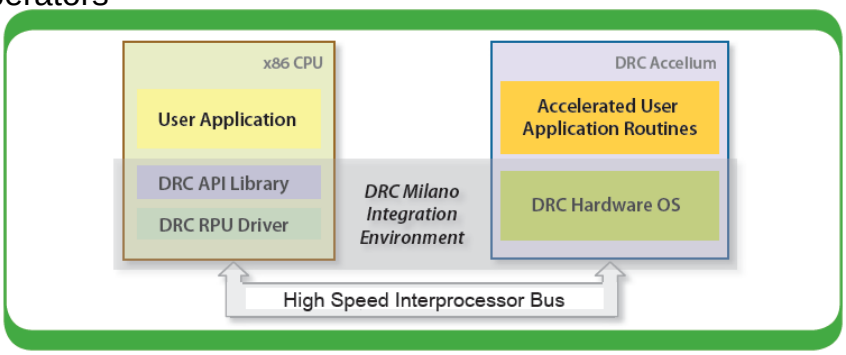
Reconfigurable Computing: In-Socket Solutions

- Accelium fits into a standard AMD Opteron Socket F slot and supports the AMD Direct Connect Architecture providing very low latency transfers directly to motherboard memory unencumbered by intermediate memory controllers.
  - Internal memory bandwidth in excess of 1 TB/s
  - External memory bandwidth of 15 GB/s
  - Low power with maximum consumption of 40 watts
  - Xilinx Virtex-5 FPGA with up to 330,000 logic cells and 576 x 18 kbits Block RAMs

http://www.drccomputer.com

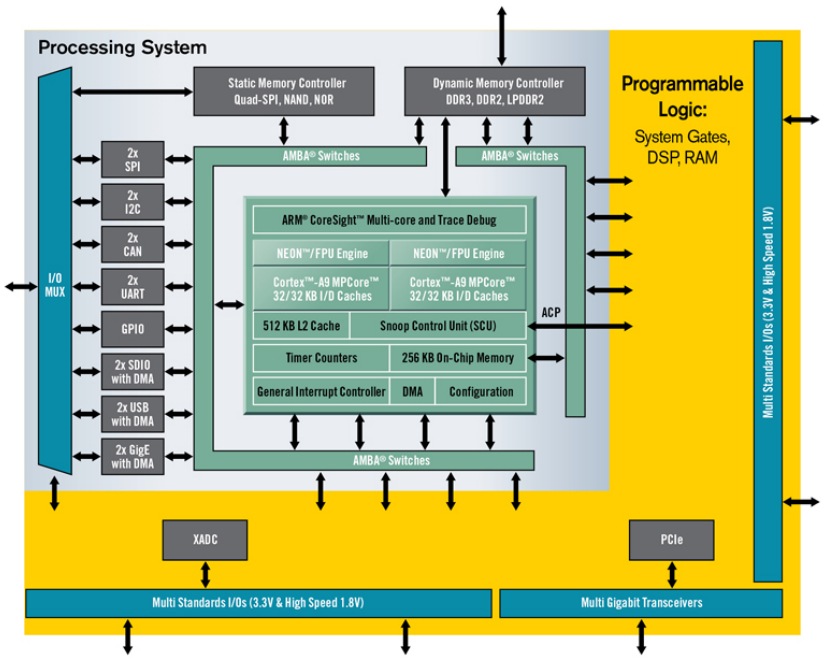
DRC's Accelium (cont.)

- Coprocessor routines are available to co-resident x86 based applications through the DRC API.
- Frequently reducing iterative processes to single cycle operations.
  - Replication in its massively parallel architecture.
  - Right-size operators to any data width
  - Multi-input operators
  - Pipelining



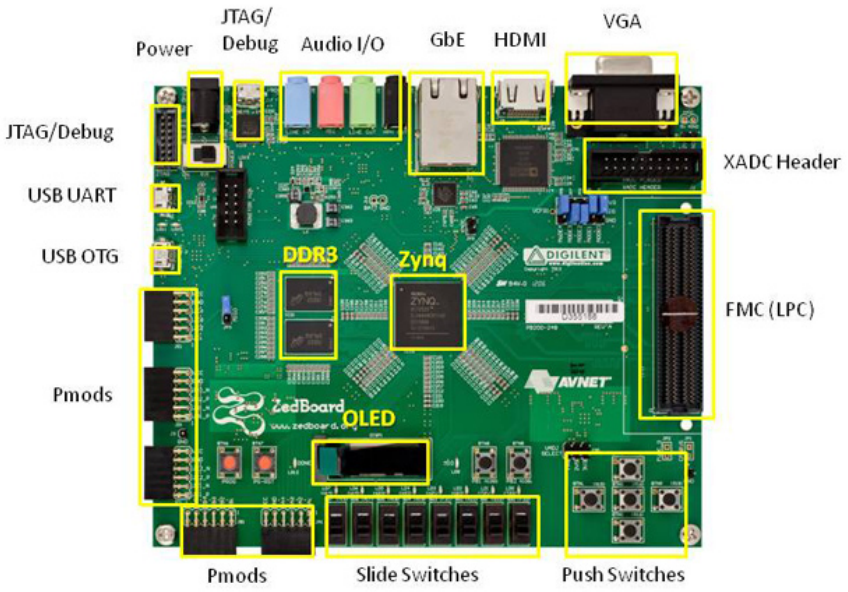
Reconfigurable Computing: Embedded Systems

- At the end of the 90's (0.25 um), FPGAs were big enough to hold processors inside themselves
  - Hard Cores: Power PC (Xilinx), Cortex-M3 (Actel).
  - Soft Cores: Nios II (Altera), MicroBlaze (Xilinx).



Zynq-7000 Extensible Processing Platform – www.xilinx.com

Xilinx's Zynq 7000



http://zedboard.org (USD 300)

* SD card cage and QSPI Flash reside on backside of board

Reconfigurable Computing: HPRC

- High-Performance Reconfigurable Computing
  - Idea appeared at the beginning of the 2000s
- Basic concepts:
  - Optimize the accelerator, especially the FPGA – processor interface
  - Use classic HPC parallelism techniques

First HPRC SRC-6e
http://www.srccomp.com

Challenges of Reconfigurable Computing

- The biggest challenge of RC is to avoid that the development costs eclipse the potential benefits
  - Non-despicable development time to port algorithms to HW.
  - Hard-to-find and expensive FPGA engineers.
  - *If development time is added to the execution time, there is no speedups.*
- **Better tools** are needed
  - The final goal is to make the underlying hardware (processor and FPGA accelerator) **transparent** to the user
  - FPGA accelerator design is already well-established (almost 20 years of history).

Challenges of Reconfigurable Computing

- HPRC market is not big enough to make viable the development of HPRC-specific reconfigurable devices
  - Tools must cope with commercial FPGA architectures
  - Same happens with processors: Big HPC machines use the same Pentiums and Cells than desktop computers and Playstations

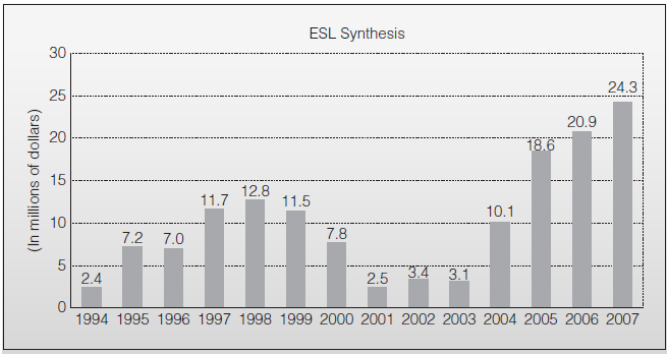


Figure A. Sales of electronic system-level synthesis tools. (Source: Gary Smith EDA statistics.)

Grant Martin, Gary Smith, "High-Level Synthesis: Past, Present, and Future," IEEE Design and Test of Computers, vol. 26, no. 4, pp. 18-25, July/Aug. 2009

Challenges of Reconfigurable Computing

- Synthesis from high-level languages already provides a moderate HW/SW unification
  - Handel-C, Impulse, SRC Map-C, Mitrion-C, etc.

Ian Page holding a Reconfigurable Computer built by Celoxica (1996?), a spin-off from Oxford University (Handel-C).

M.Sc. Ian Page short bio

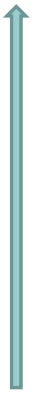
- Pre-history
- Oxford University (-1996)
- Celoxica.
- Currently:
  - Visiting professor at Imperial College London (http://www.doc.ic.ac.uk/~ipage/).
  - Independent consultant and entrepreneur (http://sevenspires.co.uk, Investment for high growth technology companies).
    - "Our remit, although simple, is a fairly tight one. We will not proceed with an opportunity where there is not believable growth to a $100m+ company, or where there is a lack of strongly defensible IP or where the valuation or amount sought is too high."

Synthesis from High-Level Languages

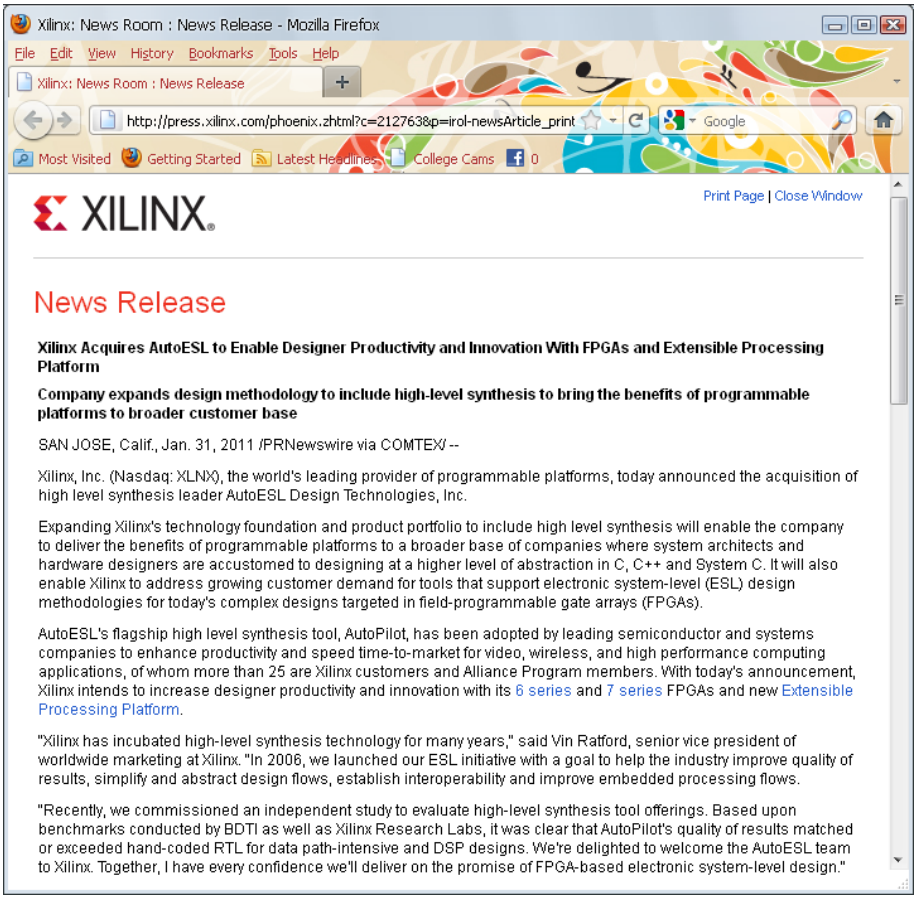
- Many benefits:
  - Improved development time
  - Less HW skills required
  - Ease the partitioning process
- Tools most commonly used:
  - Mentor Catapult (ANSI C, System-C),
  - Handel-C (ex Celoxica)
  - Synopsys Synphony HLS (earlier Synfora)
  - Cadence C-to-Silicon Compiler
  - Impulse-C (ANSI C)
  - Xilinx, earlier Auto ESL (C, C++, SystemC)
  - Altera (OpenCL)
  - DSPLogic (Simulink)
  - BlueSpec (SystemVerilog)

Different Levels of Synthesis Abstraction

More abstract, less implementation-specific



1. MATLAB Domain (pure algorithmic, non-implementation-specific)
   - m language (MATLAB)
2. Untimed C Domain (non-implementation-specific)
   - Standard C/C++
3. Timed C Domain (Implementation-specific)
   - Handel-C, System-C, SystemVerilog
4. RTL Domain (Implementation-specific)
   - Verilog, VHDL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News Release
Xilinx Acquires AutoESL to Enable Designer Productivity and Innovation With FPGAs and Extensible Processing Platform
Company expands design methodology to include high-level synthesis to bring the benefits of programmable platforms to broader customer base
SAN JOSE, Calif., Jan. 31, 2011 /PRNewswire via COMTEX/ --
Xilinx, Inc. (Nasdaq: XLNX), the world's leading provider of programmable platforms, today announced the acquisition of high level synthesis leader AutoESL Design Technologies, Inc.
Expanding Xilinx's technology foundation and product portfolio to include high level synthesis will enable the company to deliver the benefits of programmable platforms to a broader base of companies where system architects and hardware designers are accustomed to designing at a higher level of abstraction in C, C++ and System C. It will also enable Xilinx to address growing customer demand for tools that support electronic system-level (ESL) design methodologies for today's complex designs targeted in field-programmable gate arrays (FPGAs).
AutoESL's flagship high level synthesis tool, AutoPilot, has been adopted by leading semiconductor and systems companies to enhance productivity and speed time-to-market for video, wireless, and high performance computing applications, of whom more than 25 are Xilinx customers and Alliance Program members. With today's announcement, Xilinx intends to increase designer productivity and innovation with its 6 series and 7 series FPGAs and new Extensible Processing Platform.
"Xilinx has incubated high-level synthesis technology for many years," said Vin Ratford, senior vice president of worldwide marketing at Xilinx. "In 2006, we launched our ESL initiative with a goal to help the industry improve quality of results, simplify and abstract design flows, establish interoperability and improve embedded processing flows.
"Recently, we commissioned an independent study to evaluate high-level synthesis tool offerings. Based upon benchmarks conducted by BDTI as well as Xilinx Research Labs, it was clear that AutoPilot's quality of results matched or exceeded hand-coded RTL for data path-intensive and DSP designs. We're delighted to welcome the AutoESL team to Xilinx. Together, I have every confidence we'll deliver on the promise of FPGA-based electronic system-level design."


EET Synopsys buys Synfora assets
EET http://www.eetimes.com/electronics-news/4200083/Synopsys-buys-Synfo
Google
Most Visited Getting Started Latest Headlines College Cams 0
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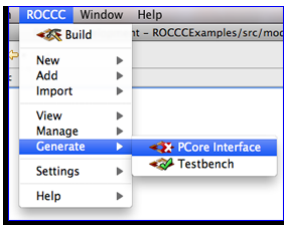
Synopsys buys Synfora assets
Dylan McGrath
6/10/2010 5:56 PM EDT
SAN FRANCISCO—In its second major acquisition announcement of the day, EDA and IP vendor Synopsys Inc. said Thursday (June 10) it has acquired technology, engineering resources and other assets of high-level synthesis EDA vendor Synfora Inc. The financial terms of the deal, which closed Thursday, were not disclosed.
Earlier Thursday, Synopsys (Mountain View, Calif.) said it signed a definitive agreement to acquire IP provider Virage Logic Inc. for $315 million in cash.
Synfora (Mountain View) provides C/C++ high-level synthesis tools used to design complex systems-on-chips (SoCs) and FPGAs. Synopsys said the deal would strengthen its position in system-level design and verification and enhance the company's FPGA-based prototyping solutions.
"This acquisition adds proven C/C++ high-level synthesis technology to our system-level solutions portfolio and broadens Synopsys' comprehensive solutions for block creation and optimization," said Joachim Kunkel, senior vice president and general manager of the Solutions Group at Synopsys, in a statement.
Synopsys did not breakdown the specifics of the acquisition or say how many Synfora employees would join the company as a result of the deal. A spokesperson for Synopsys emphasized that the deal involves Synfora's high-level synthesis tool as well as other select assets, including a "really strong" engineering team.
Brett Cline, vice president of marketing and sales at Forte Design Systems, one of the market leaders in high-level synthesis, said Synfora has not been competitive with the rest of the high-level synthesis market for some time due to its ANSI-C based technology, which he said has some fundamental limitations and is primarily focused on prototyping as opposed to real hardware design. Ultimately this resulted in an asset sale, Cline said.
Give Feedback

Open Source Tools?

- Yes…
  - ROCCC 2.0, University of California Riverside (http://www.jacquardcomputing.com/roccc/)
  - PandA, Politecnico di Milano (Italy) (http://panda.dei.polimi.it/)
  - FpgaC, historical roots at from University of Toronto (http://sourceforge.net/projects/fpgac)
  - Etc.



More info

- Boards/Platforms:
  - www.annapmicro.com
  - www.gidel.com
  - www.avnet.com
  - www.dinigroup.com
  - http://www.drccomputer.com
  - http://zedboard.org

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