ISE 12 In-depth Tutorial

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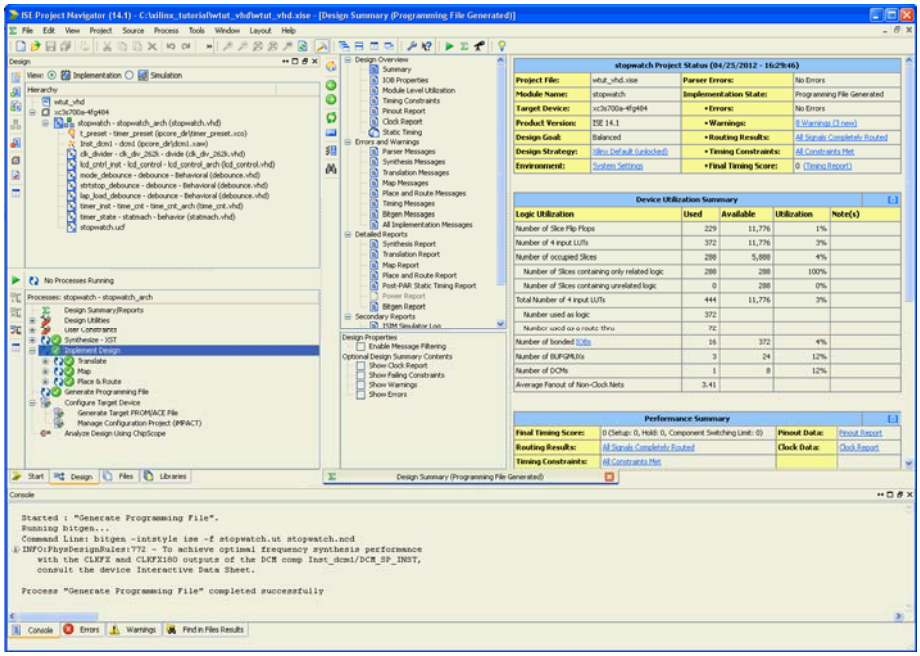
Project Navigator

1. Toolbar
2. Design Panel
3. Workspace
4. Console Panel



Design Panel

- The Design Panel displays the elements included in the project.
  - View
  - Hierarchy and
  - Processes pane
- The Processes pane displays available processes for the currently selected source.
- When you select a process, the software automatically runs the processes necessary to get to the desired step.
- The status of each process is displayed on the process icon as a red x, yellow exclamation, or green check mark.
- It's possible to view a running log of command line arguments used on the current project, expand **Design Utilities** and select **View Command Line Log File.**

Workspace

- The Design Summary lists high-level information about your project, including
  - Overview information,
  - A device utilization summary,
  - Performance data gathered from the Place & Route (PAR) report,
  - Constraints information, and
  - Summary information from all reports with links to the individual reports.

Console Panel

- The Transcript window displays
  - Status messages,
  - Errors, and warnings
  - Also contains an interactive tabs for Tcl scripting and
  - The Find in Files function.
- You can navigate from a synthesis error or warning message
  - To the location of the error in a source HDL file.
  - To Answer Records on the Support page of the Xilinx® website.

The ISE Project File

- The ISE project file (.xise extension) is an XML file:
  - ISE software version information
  - List of source files contained in the project
  - Source settings, design and process properties
- The ISE project file does not contain the following:
  - Process status information (.gise)
  - Command history
  - Constraints data

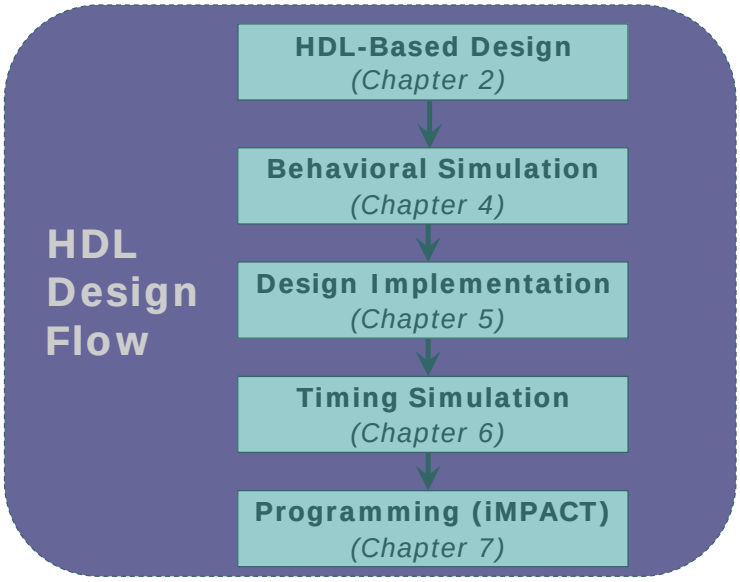
The Project Browser

- The Project Browser, accessible by selecting **File > Project Browser** provides a way to:
  - Compare multiple projects.
  - View Design Summary and Reports for a selected project before opening the project.
  - Compare detailed information for two projects.
  - Open a selected project
    - in the current Project Navigator session.
    - in a new Project Navigator session.

Tutorial Overview

- The primary focus of this tutorial is to show the relationship among
  - The design entry tools,
  - Xilinx and third-party tools, and
  - The design implementation tools in Xilinx ISE.
- There are several tutorial flows available. We will focus on the HDL flow (VHDL) (Ch. 2, 4, 5, 6, and 7).

The HDL design flow



The HDL design flow

- Chapter 2, “HDL-Based Design”
- Chapter 4, “Behavioral Simulation”
  - How to use ModelSim to simulate a design before the design implementation step.
- Chapter 5, “Design Implementation”
  - How to Translate, Map, Place and Route, and generate a .bit file.
- Chapter 6, “Timing Simulation”
  - Timing simulation with Modelsim using block and routing delay information.
- Chapter 7, “iMPACT Tutorial”
  - How to program a device with a the iMPACT configuration tool.

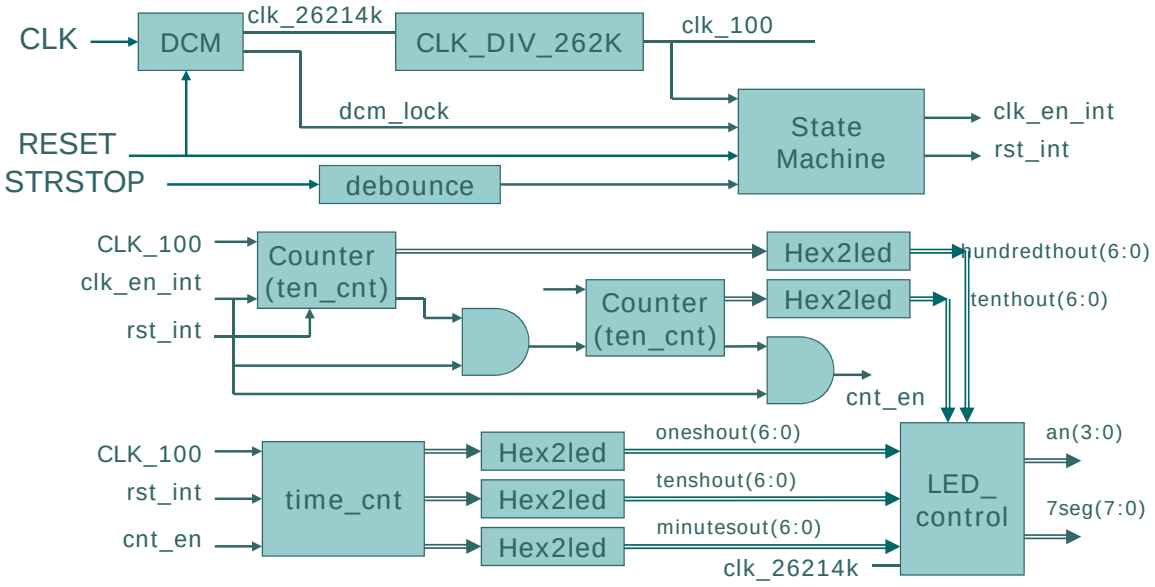
Design Description

- The design used in this tutorial is a hierarchical, HDL-based design.
- The lower-level macros are either HDL modules or CORE Generator modules.
- The design begins as an unfinished design.
- When the design is complete, you simulate it to verify the design's functionality.
- The Watch design is a simple runner's stopwatch. There are:
  - Three external inputs, and
    - The system clock is an externally generated signal.
  - Two external output buses in the completed design.

Runner's stopwatch I/O

- **Inputs**
  - **STRTSTOP** — Starts and stops the stopwatch. This is an active low signal which acts like the start/stop button on a runner's stopwatch.
  - **RESET** — Resets the stopwatch to 00.0 after it has been stopped.
  - **CLK** — Externally generated system clock.
- **Outputs**
  - **SEG_A, SEG_B, SEG_C, SEG_D, SEG_E, SEG_F, SEG_G, SEG_DP -** These outputs drive the individual segments and the decimal point for all four digits of the stopwatch design. The digits of the stopwatch are displayed on 7-segment LED displays.
  - **AN[3:0]** - This is a one-hot vector signal which drives the anodes of the four 7-segment LED displays to determine which display will be lighted.

Runner's stopwatch basic Block Diagram



Runner's stopwatch modules

- **CLK_DIV_262k:** Macro which divides a clock frequency by 262,144 (2^18).
- **DCM1:** Clocking Wizard macro with internal feedback, frequency controlled output and duty cycle correction. Converts a 50 MHz clock to a 26.2144 MHz.
- **DEBOUNCE:** HDL-based macro implementing a simplistic debounce circuit for the STRTSTOP input signal.
- **HEX2LED:** HDL-based macro. This macro decodes the ones and tens digit values from hexadecimal to 7-segment display format.

Runner's stopwatch modules

- **LED_CONTROL:** Module controlling the data multiplexing to the four 7-segment LED displays.
- **STATMACH:** State Machine module defined and implemented in StateCAD.
- **TEN_CNT:** CORE Generator™ 4-bit binary encoded counter. This macro outputs a 4-bit code which is decoded to represent the tenths and hundredths digit.
- **TIME_CNT:** Module which counts from 0:0 to 9:59 decimal. This macro has three 4-bit outputs, which represent the minutes and seconds digits.

Design Entry

- In this hierarchical design, you will examine HDL files, correct syntax errors, create an HDL macro, and add a CORE Generator module.
- With wtut_vhd project open in Project Navigator, the Sources in Project window displays all of the source files currently added to the project, with the associated entity or module names. In the current project, smallcntr and hex2led are instantiated, but the associated entity or module is not defined in the project.
- Instantiated components with no entity or module declaration are displayed with a red question-mark.

Lab1…

- The HDL Design flow, Following:
  - **“HDL-Based Design”** *(Chapter 2)*

Behavioral Simulation

- Required files
  - Design files
  - Test bench file
  - Xilinx simulation libraries
    - Required when any Xilinx primitive is instantiated in the design

Xilinx Simulation Libraries

- To simulate designs that contain instantiated
  - Xilinx primitives
  - CORE Generator components
- Update the libraries
  - Modelsim XE
    - Download the precompiled model
  - Modelsim SE
    - Compile with the `compxlib` command
      - E.g. C:\>compxlib -s mti_se -l all -f all
        -o c:\modeltech_6.2b\xilinx_libs
        -p c:\modeltech_6.2b\win32
    - Update modelsim.ini
  - Xilinx ISE Simulator
    - Automatic update

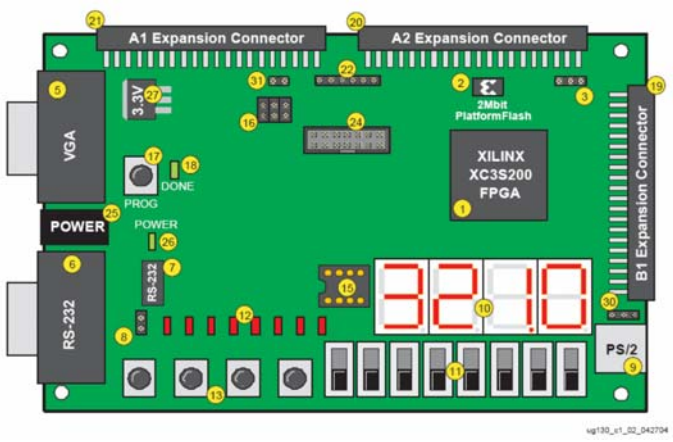
Lab2…

- The HDL Design flow, Following:
  - **“Behavioral Simulation”** *(Chapter 4)*
  - **“Design Implementation”** *(Chapter 5)*
  - **“Timing Simulation”** *(Chapter 6)*

Lab3: Fit in Starter Kit Board

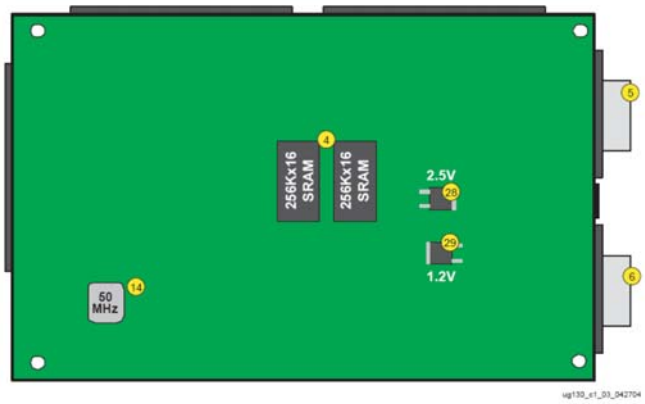
200,000-gate Xilinx Spartan-3 XC3S200 FPGA in a 256-ball thin Ball Grid Array package (**XC3S200FT256**)
♦ 4,320 logic cell equivalents
♦ 12 18K-bit block RAMs (216K bits)
♦ 12 18x18 hardware multipliers
♦ Four Digital Clock Managers (DCMs)
♦ Up to 173 user-defined I/O signals

Lab3: Starter Kit Board



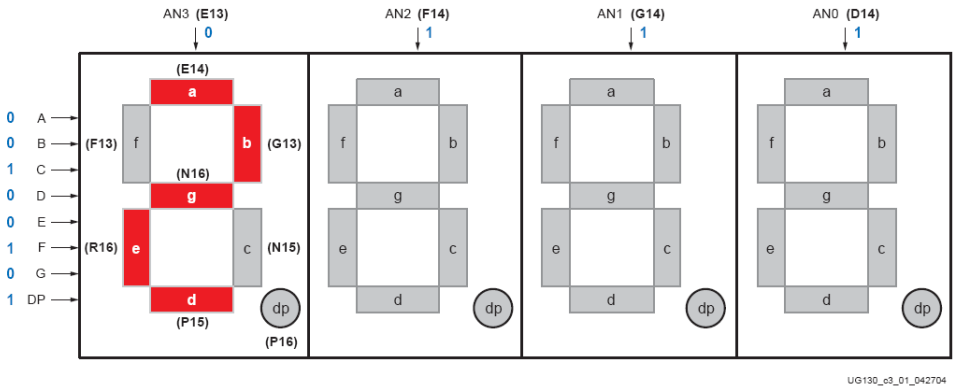
• 2Mbit Platform Flash, in-system programmable configuration PROM (2).
• PS/2-style mouse/keyboard port (9).
• Four-character, seven-segment LED display (10).
• 8 slide switches (11).
• 8 individual LED outputs (12).
• 4 momentary-contact push button switches (13).
• Push button switch to force FPGA reconfiguration (17)
• LED indicates when FPGA is successfully configured (18).
• JTAG port (22).

Lab3: Starter Kit Board



- 1M-byte of Fast Asynchronous SRAM (4).
- 3-bit, 8-color VGA display port (5).
- 9-pin RS-232 Serial Port (6).
- 50 MHz crystal oscillator clock source (14).

Starter Kit Board: Four-Digit, Seven-Segment LED Display



Starter Kit Board: Push Button Switches

Table 4-2: **Push Button Switch Connections**

Push Button	BTN3 (User Reset)	BTN2	BTN1	BTN0
FPGA Pin	L14	L13	M14	M13

- Pressing a push button generates a logic **High** on the associated FPGA pin.
- There is no active debouncing circuitry on the push button.
- The left-most button, BTN3, is also the default User Reset pin.

Starter Kit Board: Clock Sources

Table 8-1: **Clock Oscillator Sources**

Oscillator Source	FPGA Pin
50 MHz (IC4)	T9
Socket (IC8)	D9

The Spartan-3 Starter Kit board has:
- a dedicated 50 MHz clock oscillator source and
- an optional socket for another clock oscillator source.

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